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INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Use as many sheets as necessary)		Application Number	10/661,295		
		Filing Date	9/12/2003		
		First Named Inventor	Poechmueller		
		Art Unit	2812		
		Examiner Name	TBD		
Sheet	1	of	1	Attorney Docket Number	INTECH 3.0-102 03 P 51716

NON PATENT LITERATURE DOCUMENTS			
Examiner Initials*	Cite No.	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T ²
HR	1	ALLAN, G., et al., "An Yield Improvement Technique for IC Layout Using Local Design Rules," IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, November 11, 1992, pp. 1355-1362, Vol. 11, No. 11.	
HR	2	BAMJI, C., et al., "Enhanced Network Flow Algorithm for Yield Optimization," Proc Des Autom Conf; Proceedings - Design Automation Conference, June 3, 1996, pp. 746-751.	
HR	3	MALY, W., et al., "Design for Manufacturability in Submicron Domain," Computer-Aided Design, IEEE/ACM International Conference on San Jose, CA, November 10-14, 1996, pp. 690-697.	
HR	4	CHOTIN, E., et al., "A Design Planner Including a Fast Predictive Floorplanning Tool," Euro ASIC '90, May 29, 1990, pp. 208-213, Paris, France.	

Examiner Signature	<i>Yulien Rosashe</i>	Date Considered	10/26/05
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